REMARKS

Claims 1-9 and 12 are pending in this application. The Examiner rejected Claims 1-9 under 35 U.S.C. § 102(b) and objected to Claims 6 and 9. New Claim 12 was added.

Claim Objections

The Applicant has amended Claims 6 and 9 to correct a typographical error so that "trough" has been replaced by "through".

Jambotkar Does Not Anticipate the Invention of Claims 1-9

Claims 1-9 were rejected under 35 U.S.C. 102(b) as anticipated by U.S. Patent No. 4,264,857 to Jambotkar ("*Jambotkar*"). This rejection is traversed for the reasons discussed below.

Claim 1

The semiconductor device of Claim 1 requires a first semiconductor region of a first conductivity type and a second semiconductor region of the first conductivity type being in contact with the first semiconductor region.

Jambotkar completely fails to disclose a second semiconductor region of a first conductivity type being in contact with the first semiconductor region. In Fig. 2A of *Jambotkar*, the region 14 is not in contact with the region 16, because the region 14 is used as a source region while the region 16 is used as the drain region of a field effect transistor (see Column 2, lines 21-24). The region underneath the gate oxide layer 18 comprises the surface portion of the region 12 and forms the channel region 20 between the source region 14 and the drain region 16 (see Column 2, lines 34-36).

Furthermore, the semiconductor device of Claim 1 requires a fourth semiconductor region having first and second inner surfaces being in contact with first and second side

boundary surfaces of the first semiconductor region, the fourth semiconductor region being disposed between the second and third semiconductor regions.

Jambotkar completely fails to disclose a fourth semiconductor region having inner surfaces in contact with the side boundary surfaces of the first semiconductor region, the fourth semiconductor region being disposed between the second and third semiconductor regions. In Fig. 2A of *Jambotkar*, the inner surface of the region 10 never contacts the side boundary surface of the region 16, because the region 12 is inserted between the region 10 and the region 16. Moreover, the region 10 is not disposed between the region 14 and the region 12, which is required by Claim 1.

Accordingly, *Jambotkar* does not anticipate Claim 1.

Claims 2-9

Claims 2-9 depend from independent Claim 1. The remarks made above in support of independent Claim 1 are equally applicable to distinguish the dependent claims from *Jambotkar*.

Claim 12

New Claim 12 is supported at least by the embodiment of Fig. 5 and the accompanying text. Claim 12 is not anticipated by *Jambotkar*. As discussed above in more detail in connection with Claim 1, *Jambotkar* does not describe a fourth semiconductor region having inner surfaces in contact with the side boundary surfaces of the first semiconductor region. Nor does *Jambotkar* describe a second semiconductor region configured as required by Claim 12.

CONCLUSION

The foregoing is submitted as a complete response to the Office Action identified above. This application should now be in condition for allowance, and the Applicant solicits a notice to that effect. If there are any issues that can be addressed via telephone, the Examiner is asked to contact the undersigned at 404.685.6799.

Respectfully submitted,

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